

Please add the following claims:

- Ar
- Sub B4
- 1 --21. A computer readable medium comprising instructions for a
2 computer implemented chip design method, said method comprising
3 the steps of:
4 a) retrieving a wire width constraint from technology data
5 for an I/O cell;
6 b) retrieving a maximum resistance constraint from said
7 technology data for said I/O cell;
8 c) propagating said wiring width constraint and said
9 maximum resistance constraint to net design data for said chip;
10 d) generating said chip, connections between said I/O cell
11 and an associated pad being constrained by said propagated
12 constraints; and
13 e) checking said wired integrated circuit.

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- 1 22. The computer readable medium comprising instructions as
2 recited in claim 21, wherein a plurality of I/O cells are wired and further
3 comprising before the checking step (e), repeating steps (a) - (d) for
4 each of said plurality of I/O cells.

- Sub B5
- 1 23. The computer readable medium comprising instructions as
2 recited in claim 22, further comprising before the checking step (e), the
3 step of:
4 d1) wiring any unused chip pads to a cell including a
5 connection to power rail or to a power return rail.

- 1 24. The computer readable medium comprising instructions as
2 recited in claim 22, further comprising before the checking step (e), the
3 step of:
4 d1) wiring any unused chip pads to a cell including an ESD
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